

ABSTRACT

A process for forming an isolation region comprised of shallow trench - deep trench configuration, wherein a smooth top surface topography is obtained for the isolation region and for adjacent active device regions in the semiconductor substrate, has been developed. The process features initially forming an insulator filled shallow trench shape, planarized via a first chemical mechanical polishing procedure, allowing reduced complexity to be realized during the subsequent formation of a narrow diameter, deep trench opening, in the insulator filled shallow trench shape and in an underlying portion of semiconductor substrate. Formation of a recessed polysilicon plug located in the bottom portion of the deep trench opening is followed by formation of an insulator plug located in a top portion of the deep trench opening, overlying the recessed polysilicon plug. This is accomplished via photolithographic and selective dry definition procedures, and a second chemical mechanical polishing procedure, resulting in a filled, deep trench opening exhibiting a smooth top surface topography.